

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A fabrication method for integrating a plurality of heterogeneous circuit devices in a single substrate, comprising:

providing a substrate;

forming a first protective layer over the substrate;

removing a portion of the first protective layer;

ion implanting a high voltage well of a first circuit device in the substrate using the partially removed first protective layer;

forming a second protective layer over the substrate;

removing a portion of the second protective layer; and

ion implanting a first low voltage well of a second circuit device in the substrate using the partially removed second protective layer.

2. (Original) The method of claim 1, further comprising ion implanting a photodiode in the substrate.

3. (Original) The method of claim 1, further comprising forming at least one microelectromechanical system-based element in the substrate.

4. (Original) The method of claim 1, wherein providing a substrate comprises providing a layer of silicon.

5. (Original) The method of claim 4, wherein providing a layer of silicon comprises providing a layer of p-type silicon.

6. (Original) The method of claim 1, wherein providing a substrate comprises providing a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

7. (Original) The method of claim 6, wherein providing a silicon-on-insulator wafer comprises providing a silicon-on-insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

8. (Original) The method of claim 1, further comprising:

forming a third protective layer over the substrate;

removing a portion of the third protective layer; and

ion implanting a second low voltage well of the second circuit device in the substrate.

9. (Original) The method of claim 8, further comprising forming a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

10. (Original) The method of claim 8, further comprising ion implanting the substrate to adjust a threshold of the high voltage well, the first low voltage well and the second low voltage well.

11. (Currently Amended) The method of claim 9, further comprising:

forming a polysilicon layer over ~~the a~~ gate oxide and the field oxide layer; and

removing a portion of the polysilicon layer to define a polysilicon gate for each of the high voltage well, the first low voltage well and the second low voltage well.

12. (Original) The method of claim 11, further comprising:

forming a fourth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fourth protective layer; and

ion implanting a P-body in the high voltage well of the first circuit device using the partially removed fourth protective layer.

13. (Currently Amended) The method of claim 12, further comprising:

forming a fifth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fifth protective layer; and

ion implanting at least one N⁺ source/drain in the P-body, in the high voltage well of the first circuit device and in the first low voltage well of the second circuit device using the partially removed fifth protective layer.

14. (Currently Amended) The method of claim 13, further comprising:

forming a sixth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the sixth protective layer; and

ion implanting at least one P⁺ source/drain in the P-body and in the ~~second-first~~ low voltage well of the second circuit device using the partially removed sixth protective layer.

15. (Original) The method of claim 14, further comprising forming a passivation oxide layer over at least the field oxide layer and the polysilicon gates.

16. (Original) The method of claim 15, further comprising:

forming a plurality of vias through the passivation oxide layer to each of the N⁺ and P⁺ sources/drains;

forming a layer of metal over the passivation oxide layer and in the vias; and

removing a portion of the layer of metal over the passivation oxide layer to define a plurality of electrical interconnects.

17-28. Canceled

29. (Currently Amended) A fabrication method for a heterogeneous device, comprising:

providing a substrate; and

successively masking, ion implanting, oxidizing, thin film depositing and annealing the substrate to define a plurality of heterogeneous circuit devices in the substrate;

wherein the ion implanting is accomplished using at least two successive masks.

30. (Original) The method of claim 29, further comprising forming at least one microelectromechanical system-based element in the substrate.

31. (Original) The method of claim 29, wherein masking the substrate comprises: forming a protective layer; and
removing a portion of the protective layer.

32. (Original) The method of claim 29, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate comprises ion implanting and annealing at least one photodiode.

33. (Original) The method of claim 29, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate comprises ion implanting at least one complementary metal oxide semiconductor transistor and at least one double-diffused metal oxide semiconductor transistor.

34. (Original) The method of claim 33, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate further comprises ion implanting and annealing at least one photodiode.

35. (Original) The method of claim 29, wherein providing a substrate comprises providing a layer of silicon.

36. (Original) The method of claim 35, wherein providing a layer of silicon comprises providing a layer of p-type silicon.

37. (Original) The method of claim 29, wherein providing a substrate comprises providing a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

38. (Original) The method of claim 37, wherein providing a silicon-on-insulator wafer comprises providing a silicon-on-insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

39-46. Canceled